TDC Transition Module for Fiber Optic Transmission

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Introduction

The TDC Transition Module for Fiber Optic Transmission is a replacement part for COT transition modules. The transition modules carry data from TDC boards to the XFT. The COT transition modules have LVDS drivers and connectors to accommodate copper Ansely cables. The replacement board will have an accompanying Four Channel Optical Transmitting Mezzanine Module. The TDC interface is the same to both transition modules. The XFT interface is quite different between them.

Hardware

Data, Strobe, Word Zero and Beam Zero signals come from the TDC P5/6 connector and are routed to an FPGA. The fpga, a Xilinx Spartan IIE, is not 5v tolerant. There is on-board flash RAM for configuration memory for the FPGA. Programmability of the FPGA and RAM is provided by a boundary scan chain composed of a JTAG header, the FPGA, and the flash RAM. The boundary scan chain is not extended to the backplane.

A differential PECL cdf_clock comes from the P2 connector. The signal is passed through a couple ICs to generate an LVTTL cdf_clock. One copy is routed to the mezzanine card and one copy is routed to the FPGA.

The transition module runs off of +5v supply from the backplane. It has three voltage regulators to generate +3.3v, +2.5v and +1.8v. The +1.8v is to drive the core section of the fpga. +2.5v is routed to the mezzanine card. +3.3v is the main supply of the transition module, including the io section of the fpga, and is routed to the mezzanine card.

There are three connectors between the transition module and the mezzanine card. The fpga drives almost all the signals through the connectors. The mezzanine card supplies a clock signal, which indicates the transmission rate of data for its fiber optic transmitter. This clock signal is routed to the fpga.

Firmware

The fpga serves as a translator between the TDC and the mezzanine card. Data entering the fpga from the TDC will arrive every 22ns. This data is repackaged into a format with a clock rate of ~16.5ns. See “Run Iib TDC Upgrade: New TDC Implementation in the XFT” for the input
format. See “A Four Channel Optical Receiver Mezzanine Module and A Four Channel Optical Transmitter Mezzanine Module” for the output format.

Data will probably be sent in 24-word contiguous packets. If a clock period of the transmitter is faster than $132\text{ns}/8$, then an extra word would be tacked onto the end of the 24-word packet, when necessary.