

The CLEO-III Trigger: Axial and Stereo Tracking¹

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Abstract

The tracking subsystem of the CLEO-III Trigger consists of separate axial and stereo tracking pattern-matching modules, whose products are time-aligned and spatially correlated to provide pipelined trigger information every 42 ns with a latency of approximately 2 μ s. This paper describes the pipelined signal processing and pattern recognition schemes used by the axial and stereo electronics to provide the information necessary to make trigger decisions. Extensive use of in-system field programmable gate arrays support path finding and timing information extraction.

I. INTRODUCTION

The CLEO-II experiment began accumulating data at the Cornell Electron Storage Ring (CESR) in 1989. Serving as a world-class facility for the study of heavy quark physics, both CLEO and CESR have undergone substantial upgrades in recent years resulting in improved performance. This paper (the second of three [1,2]) addresses the tracking aspects of the trigger for the most recently completed CLEO detector upgrade, CLEO-III.

A detailed discussion of the design parameters for the trigger and data-acquisition systems appears in the CLEO-III Detector Proposal [3], and again in the 1994 CLEO-III Detector Status Report [4]. Previous descriptions of the trigger system, written before the design was finalized, appear in the references [5,6,7]. We present a brief overview of the entire CLEO-III trigger, followed by more detailed descriptions of the axial and stereo tracking components of the trigger, as well as timing extraction from these trigger elements.

II. SYSTEM OVERVIEW

A schematic view of the CLEO-III trigger system is shown in Figure 1. Data from the calorimeter and drift chamber are received and processed in separate VME crates by the appropriate circuit boards to yield basic trigger primitives such as the track count and topology in the drift chamber, as well as the shower count and topology in the electromagnetic calorimeter. The information from both systems is correlated by global trigger circuitry which generates an L1Pass strobe every time a valid trigger condition is satisfied. The L1Pass

signals are conditionally passed by the data flow control circuitry to the gating and calibration modules for distribution to the data acquisition system. In addition, luminosity information is obtained from the digital calorimetry subsystem and provided to the CESR accelerator via the global trigger.

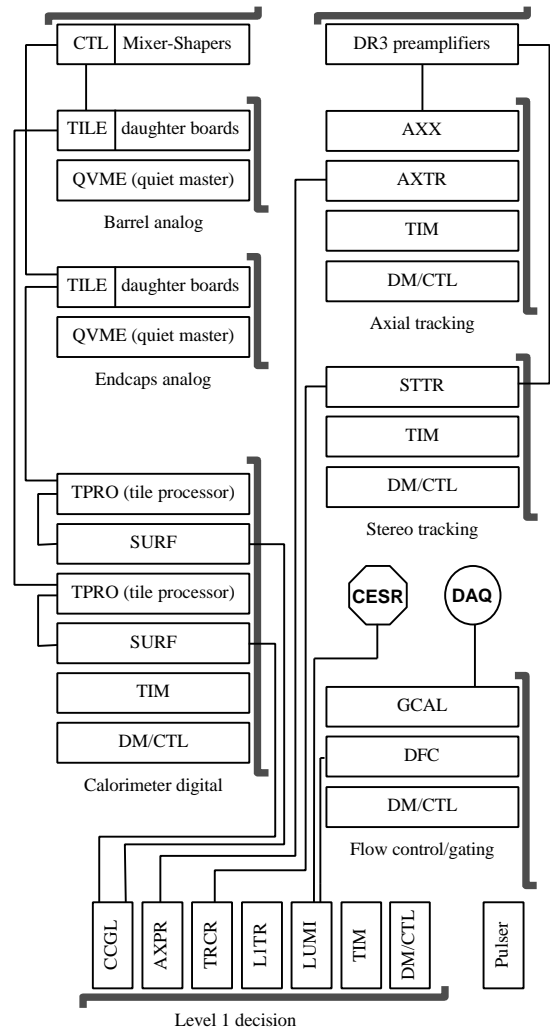


Figure 1: Overview of the CLEO-III Trigger Hardware. Not shown is the conventional VME CPU which directs the QVME interfaces.

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Details on the analog and digital calorimetry trigger can be found in the first companion paper [1], and details of the decision and gating can be found in the third companion paper [2], located elsewhere in these proceedings.

The block labeled “112 to 48” has two functions. First, it performs a clustering algorithm on the input bits such that (for example) a pair of set adjacent inputs set a single topology bit. Next, the 112 bits are merged to produce 48 bits topological information that are sent, after pipelining, to the TRCR boards. The input tracking bits are also processed by a circuitry that counts how many of the 112 bits are asserted. This calculation is pipelined, taking three “ticks” to complete, producing a valid 7 bit answer for every tick. This tick-by-tick track count information is also used to extract the event time. The algorithm to do this is discussed in Section IV.

The outputs of the AXPR board are passed through pipelines before they are presented to the P5P6 backplane in the Level 1 decision subrack. These simply act as adjustable length digital delays, and are used to time-align the various tracking trigger results with each-other, and also to align the tracking results with the high latency calorimeter information.

The clustering, merging and counting logic is implemented in a set of Altera “MAX” 7000 series ISP-FPGAs.

B. Stereo Tracking

The stereo section (layers 17-47) of the CLEO-III drift chamber differs from the axial section in that the stereo wires are offset with respect to parallel of the beam pipe; the axial wires are almost exactly parallel. It is broken up into 8 super layers. The first 7 super layers have 4 layers each; the last has only 3. The odd super layers are called the U super layers and have a positive phi tilt with respect to Z; the even ones are V super layers and have a negative tilt.

There are too many (8100) wires in the stereo section of the drift chamber for the stereo tracker to examine every wire individually. Instead, the stereo tracker receives 1 bit for every 4 by 4 blocks of wires (for super layer 8 it uses 4 wide by 3 layers tall). These bits are formed by Altera FPGAs in the drift chamber crates. As in the axial section, the FPGAs get a signal from a discriminator of width 700 ns.

The stereo tracker uses these bits to make its decisions. The U and V super layers are tracked separately since they tilt in opposite directions. The stereo trigger has therefore 2 independent components, although both are in the same crate, each looking at block patterns in their 4 super layers.

The stereo block definitions (which pattern of 4 wires turn on a block) and the stereo road definitions (which groups of U or V blocks is considered a valid track) were generated from simulated tracks having momentum transverse to the beam greater than 250 MeV/c. In order to satisfy a block pattern, a hit must be present on at least 3 out of 4 layers. This missing hit allows high track finding efficiency for realistic wire efficiencies. Stereo roads, however, do not allow for missing blocks.

The output of the stereo tracker is 2 projections. The first points inward towards which layer 9 wires the track could have passed through, breaking up the layer 9 wires into 48 sections, as well as if the track is caused by a low momentum positive particle, low momentum negative particle or high momentum positive particle. The definition of high and low is programmed in the FPGAs and can be changed easily *in situ* through the board’s

VME interface. The second points to where the track is projected to have hit the crystal calorimeter with a resolution of 24 sections. Due to the tilt of the stereo section of the drift chamber, a single stereo road will in general activate several layer 9 sectors and possibly multiple calorimeter sectors.

One stereo tracking (STTR) board is responsible for both the inputs and outputs for one-sixth of the drift chamber for U or V (12 boards total). Each STTR board uses 5 Altera 8820 FPGA to perform the pattern lookup for the stereo roads. To prevent inefficiencies at board boundaries, both inputs (blocks) and outputs (layer 9 and CC projections) must be shared between neighboring STTRs. This is also done on a custom J5/J6 backplane. Each board uses 5 Altera 7128 FPGAs and 1 Altera 7192 FPGA to route incoming, outgoing and shared signals. Because of the flexibility of the FPGAs, we only needed 1 board design even though there are 4 distinct board types (2 for U and 2 for V). As with the axial tracker, pattern recognition is performed for the entire stereo portion every 42 ns. The outputs from each STTR are sent via LVDS to the tracking correlator for further processing.

The stereo tracking trigger provides high efficiency per track, and good background rejection. An important lesson from CLEO-II has been that modeling backgrounds can be very difficult. The stereo tracking trigger is sensitive to backgrounds than the inner axial tracking trigger, and will be crucial in providing a high overall rejection factor.

C. Tracking Correlation

The results from the 16 axial tracking boards are combined with the product of the stereo trigger in the tracking correlator (TRCR). The TRCR function is implemented on two 9Ux400mm VME circuit boards, each handling half of the input information. A block diagram of the TRCR system is shown in Figure 4.

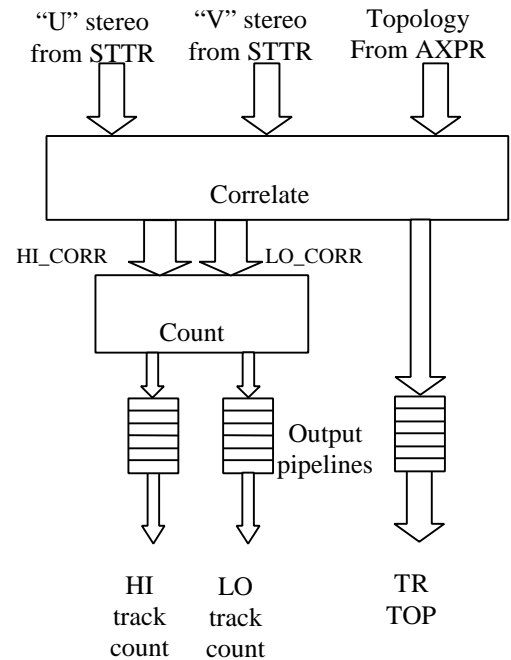


Figure 4: TRCR Logic Diagram

The STTR receives azimuthal projection information from both U and V stereo super layers. This information consists of 48 “positive” bits, 48 “negative” bits and 24 “CC” bits for each of U and V.

As discussed in the previous section, the positive and negative bits carry information about the charge of the particle that made the track and about the perpendicular momentum component of this particle. If a track is classified as only positive or negative, it will be labeled as a low momentum track. If the STTR board could not determine the momentum unambiguously, then the track is labeled as a high momentum track.

Since the TRCR system also receives 48 projection bits from the AXPR, it can perform a bin by bin correlation test between the axial and stereo tracking information. In the present mode of operation there are two intermediate sets of 48 correlation bits, one each for low and high momentum tracks, and the definition for each one is simply:

$$LO_CORR_i = AXIAL_i \& (LO_STTR_U_i \# LO_STTR_V_i)$$

$$HI_CORR_i = AXIAL_i \& (HI_STTR_U_i \# HI_STTR_V_i)$$

These LO and HI output topology bits are counted to produce a LO track count and a HI track count, both of which are pipelined and placed on the P5P6 backplane in the Level 1 decision subrack.

The LO and HI bits are OR’ed bin by bin to produce an array of 48 correlated topology bits. These bits, along with the 24 “CC” bits, can be combined as desired to produce a set of 48 final correlated topology bits, which are pipelined and also placed on the P5P6 backplane. As of October 2000 the final topology bits are 24 inward track projection bits (simply ORing adjacent topology bits) and the 24 “CC” bits.

An added benefit of the tracking correlation may turn out to be its availability to the Level 3 processors. It has been proposed that the Level 3 trigger, which is performed on the fully assembled event, need not perform conventional track finding on the drift chamber data, as long as position information is available from the axial region and curvature information is available from stereo. These two pieces of information, as connected by the tracking correlator, may be sufficient for directing track-finding searches in the silicon vertex detector. This could save significant amount of Level 3 processing time. Work is in progress on evaluating this possibility.

IV. TIMING EXTRACTION

Considerable effort has been expended to understand the details of the timing behavior of the axial tracking hardware. Simulations, using CLEO-II data to generate CLEO-III tracks, indicates that for most tracks at least one wire-hit in the track will have a drift time that is short enough to be usable in determining the event time. Individual wire-hit signals are discriminated to produce fixed-width output pulses. Figure 5 shows the timing distribution produced by monitoring the track-matching FPGA, and determining when tracks become invalid. This corresponds to the removal of the first hit, which

due to the fixed pulse-width discrimination is also indicative of the first arrival time. The RMS of the shown distribution is about 12 ns.

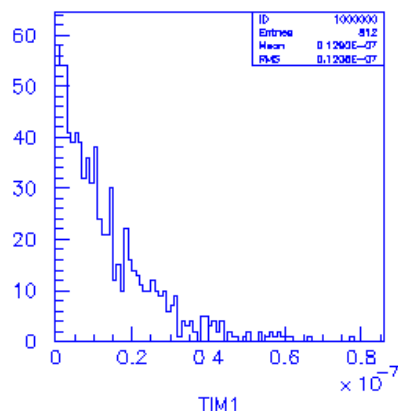


Figure 5: Time of trigger “invalid” from axial tracking.

The implementation of this algorithm in the trigger hardware (specifically, on the AXPR board) involves monitoring the tick-by-tick track count as an event evolves through the detector. A finite state machine, implemented in an Altera “MAX” 7000 series ISP-FPGA device, examines the 7 bit track count (calculated on the same board) and senses when this quantity starts to drop off after reaching a maximum, as indicated in Figure 6. This point in time will, in most cases, be exactly one discriminator width later than the arrival time of the first hit on a track, which, as seen in Figure 5, is a good measure of the event time.

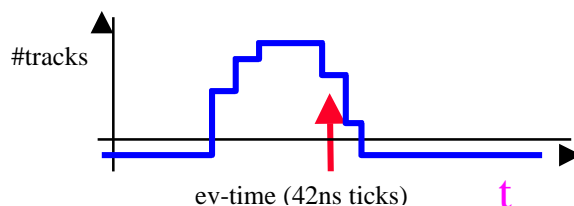


Figure 6: Time evolution of the axial track count for a typical hadronic event. The vertical arrow indicated when the timing extraction hardware fired.

This time extraction method works extremely well. Figure 7 is a plot of timing bucket (each one 42 ns wide) on the horizontal axis versus number of events on the vertical axis, for all events in an early CLEO-III era run. The timing bucket assigned to each event is extracted from the trigger based on the hardware described above. It repeats after 61 buckets since this is the number of unique 42 ns time increments that correspond to a complete revolution of a beam particle in the Cornell Electron Storage Ring (CESR), which is providing the e^+e^- collisions recorded by the CLEO-III experiment. The eight peaks correspond to the structure of the beam particles within CESR. A careful analysis of these peaks, taking into account the known underlying CESR beam structure, indicates that the resolution we achieve is in fact slightly better than we had expected based on simulation.

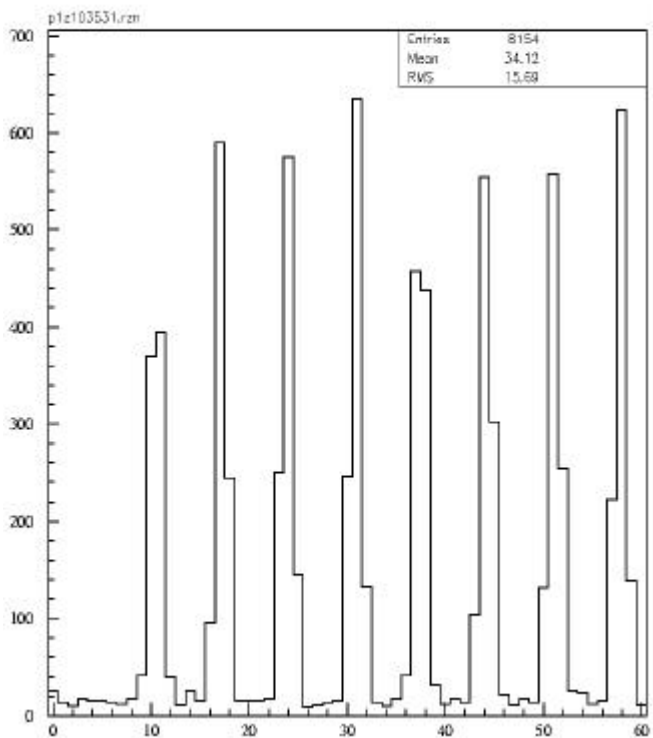


Figure 7: The beam structure of the Cornell Electron Storage Ring as recorded by the CLEO-III trigger timing extraction hardware.

- [7] Bergfeld, et al., “The CLEO-III Trigger: Decision and Gating” in the Proceedings of the 1996 Nuclear Science Symposium, Norfolk, VA, October 1996.

V. PROJECT STATUS

The axial tracking trigger was built, then installed in CLEO-III during 1999; the stereo trigger was installed during 2000. As of October, 2000 both triggers are in active use.

V. SUMMARY

The tracking elements of the CLEO-III trigger have been presented. We have described the axial and stereo logic used to draw conclusions about the pattern of charged particle tracks in the CLEO-III drift chamber.

VIII. REFERENCES

- [1] see also “The CLEO-III Trigger: Analog and Digital Calorimetry” in these proceedings.
- [2] see also “The CLEO-III Trigger: Decision and Gating” in these proceedings.
- [3] CLEO-III Detector Proposal, CLNS-94/1277. Available from Cornell University, Wilson Lab, Ithaca, NY 14853-8001.
- [4] 1994 CLEO-III Detector Status Report, CBX 94-73. Available from Cornell University, Wilson Lab, Ithaca, NY 14853-8001.
- [5] Bergfeld, et al., “The CLEO-III Trigger System,” in the Proceedings of the 1995 Nuclear Science Symposium, San Francisco, October 1995.
- [6] Bergfeld, et al., “The CLEO-III Trigger: Calorimetry and Tracking” in the Proceedings of the 1996 Nuclear Science Symposium, Norfolk, VA, October 1996.