

The CLEO-III Trigger: Analog and Digital Calorimetry¹

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Abstract

The calorimetry subsystem of the CLEO-III Trigger incorporates both analog and digital electronics to provide pipelined trigger information every 42 ns with a latency of approximately 2.5 μ s. This paper describes the pipelined signal-processing and pattern-recognition schemes used to provide calorimeter information to the experiment trigger, with somewhat greater emphasis on the analog components of the system. Analog processing is employed to address the quantization error caused by split energy deposition in adjacent calorimeter cells, and digital field programmable gate arrays are used extensively to filter and categorize the calorimeter energy topology. Timing, geographical, and energy information are all available for use in the calorimeter trigger.

I. INTRODUCTION

The CLEO-II experiment began accumulating data at the Cornell Electron Storage Ring (CESR) in 1989. Serving as a world-class facility for the study of heavy quark physics, both CLEO and CESR have undergone substantial upgrades in recent years resulting in improved performance. This paper (the first of three [1,2]) addresses the calorimetry aspects of the trigger for the most recently completed CLEO detector upgrade, CLEO-III.

A detailed discussion of the design parameters for the trigger and data-acquisition systems appears in the CLEO-III Detector Proposal [3], and again in the 1994 CLEO-III Detector Status Report [4]. Previous descriptions of the trigger system, written before the design was finalized, appear in the references [5,6,7]. We present a brief overview of the entire CLEO-III trigger, followed by more detailed descriptions of the analog and digital circuitry used to form the detector's calorimetry trigger.

II. SYSTEM OVERVIEW

A schematic view of the CLEO-III trigger system is shown in Figure 1. Data from the drift chamber and calorimeter are received and processed in separate VME crates by the appropriate circuit boards to yield basic trigger primitives such

as the track count in the drift chamber, as well as the shower count and topology in the electromagnetic calorimeter. The information from both systems is correlated by global trigger circuitry which generates an L1Pass strobe every time a valid trigger condition is satisfied. The L1Pass signals are conditionally passed by the data flow control circuitry to the gating and calibration modules for distribution to the data acquisition system. In addition, information from the trigger system is used by the CESR accelerator to monitor luminosity.

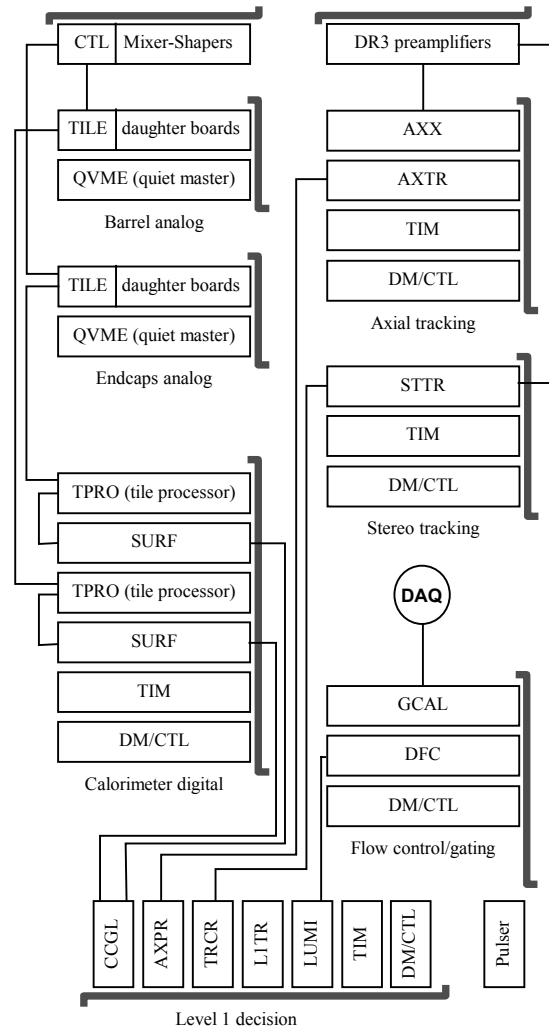


Figure 1: Overview of the CLEO-III trigger hardware. Not shown is the conventional VME CPU which directs the QVME interfaces.

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Details on the axial and stereo tracking triggers can be found in the second companion paper [1] while information about the decision and gating can be found in the third paper [2], located elsewhere in these proceedings.

III. CALORIMETRY TRIGGER

The CLEO-III calorimeter (CC) comprises 1,656 doped CsI crystals in the detector “endcaps” and 6,144 crystals in the “barrel.” The light output from a crystal turns on rapidly, then decays with a 900 ns time constant. Four photodiodes are mounted on each crystal; each photodiode is viewed by a separate charge-sensitive integrating preamplifier. Preamplifier outputs are not cleared after an event, but decay exponentially to ground with a 180 μ s time constant.

The calorimeter energy from a shower is usually shared among several crystals. As a result, the efficiency for setting a threshold bit in a particular region of the calorimeter depends both on energy and position: a 200 MeV shower shared by crystals spanning a boundary can be below threshold in both regions. Precision analyses of CLEO-II data, such as those studying τ decays, were frequently limited by systematic rather than statistical uncertainties. Contributing to the systematic errors were effects associated with Monte Carlo simulation of the tracking and CC trigger efficiencies.

To reduce the difficulties associated with simulation of the trigger, and to increase its flexibility, the CC trigger was redesigned for CLEO-III. Complications associated with boundaries in the calorimeter are reduced by creating overlapping “tiles” by forming analog sums of signals from groups of 64 CsI crystals, as shown in Figure 2. A photon striking the calorimeter will deposit nearly all of its energy in at least one of the groups of crystals summed into a tile. Naturally, a signal in a single crystal will appear in four different tiles; it is the tile processor’s task to account for this.

A diagram of the path for a single crystal’s signal through the CC trigger electronics is shown in Figure 3.

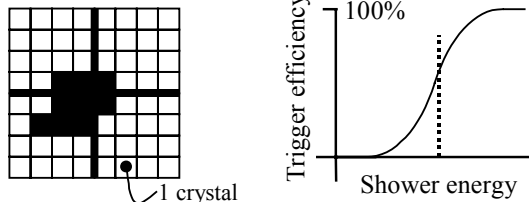
Mixer-shaper cards receive the signals from up to sixteen crystals. Signals from the four photodiodes viewing a crystal are summed by the mixer-shapers, then corrected for crystal-to-crystal gain variations. One copy of the gain-corrected signal is shaped, integrated, and passed to ADC’s for use in off-line analysis. Another copy is summed with those from the other crystals assigned to the same mixer/shaper card. This summed signal is then shaped to have 2.5 μ s leading and \sim 8 μ s trailing edges. The calorimeter uses 384 (120) mixer-shaper cards to process barrel (endcap) signals. A controller in each of the 24 mixer-shaper crates creates differential copies of the shaped signals to be sent, through shielded cables, to the tiling system (TILE). The CLEO-III calorimeter, upstream of the mixer-shaper controllers, is nearly identical to the CLEO-II CC which has been described in reference [8].

A. Daughter Board

Each mixer-shaper signal is received by a small “daughter board” which then copies it, passing the copies to neighboring daughter boards. A block diagram of a daughter board is

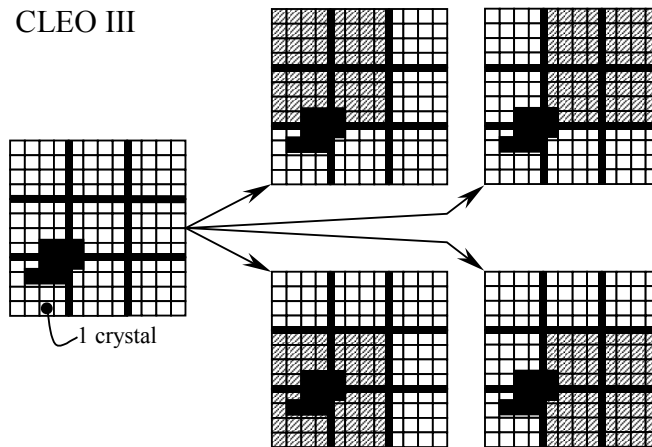
shown in Figure 4. Each is built as a small 8-layer printed circuit board, whose layout allows it to carry both analog and digital signals. Up to 24 daughter boards are mounted on each triple-width 9U \times 400mm VME board (TILE) which provides power (and other services), test pulses, and signal routing between daughter boards. The calorimeter requires 384 (120) daughter boards for barrel (endcap) crystals. Approximately 700 daughter boards were built for CLEO-III.

CLEO II



Energy splits: shared by 4 mixer-shaper cards. Hard to model...

CLEO III



Construct overlapping tiles: ≥ 1 holds energy of entire shower

Figure 2: Showers spanning boundaries between regions in the CLEO-II calorimeter were difficult to simulate precisely. The heavy lines indicate boundaries between mixer-shaper cards. For CLEO-III, which forms analog sums of overlapping regions, at least one “tile” will contain the entire shower. (The signal from each mixer-shaper contributes to four tiles.) In the drawing, (part of the) energy from one shower is included in the signals of several different (overlapping) tiles. For clarity, only the four tiles associated with the central mixer-shaper are shown.

The daughter board circuit uses Analog Devices AD8842 8-bit “TrimDACs” to adjust the gains of each of the four signals being summed. An eight-channel device, the AD8842 is, in effect, a digital-to-analog converter whose analog bandwidth at its voltage reference input is sufficiently great so that it can be used as a signal amplifier with programmable gain between -1 and $+1$. Since the manufacturer’s documentation indicates that the AD8842 bandwidth is best when running with negative gains, the daughter boards were designed to use a nominal AD8842 gain of -0.8 . This way, a

± 1 change in programmed gain data would effect a $\pm 1\%$ change in the device's analog signal gain.

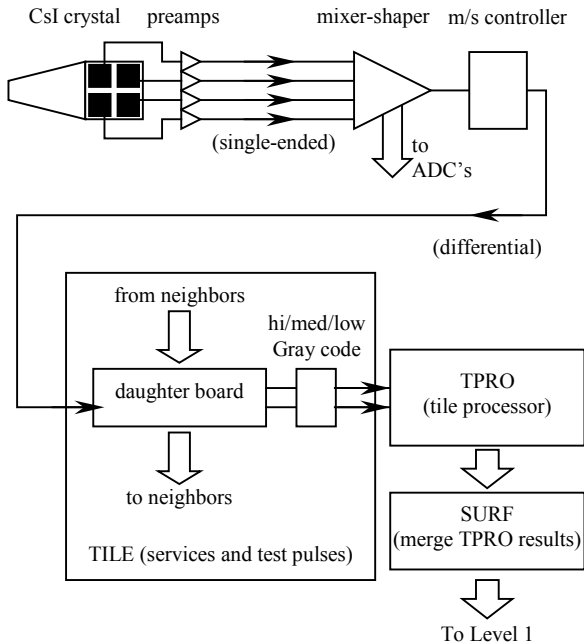


Figure 3: Signal path for one crystal. Signals from preamps peak $3 \mu\text{s}$ after formation, then return to ground with $180 \mu\text{s}$ time constant. Signals from mixer-shaper controllers are differential, peak $2.5 \mu\text{s}$ after onset, then return to ground with $\sim 8 \mu\text{s}$ time constant. A daughter board prepares copies of its mixer-shaper signal to send to neighboring boards. It then forms an analog sum of signals from four mixer-shaper cards. The summed signal is shaped into a bipolar pulse which is discriminated. For signals which exceed thresholds, logic pulses whose leading edges coincide with zero-crossings of the bipolar pulses are sent to the tile processors. Results from the system's tile processors are combined by the SURF boards, then sent to the Level 1 trigger.

Pulse shaping after the four-channel sum produces a bipolar signal with a negative peak at 700 ns , a zero-crossing at $1.4 \mu\text{s}$, and a positive peak at $2 \mu\text{s}$, followed by a relatively gentle return to ground. The bipolar signal is passed to three discriminator subcircuits built around Maxim MAX912 comparators. The MAX912 is well behaved for small overdrives—it does not tend to oscillate when its signal and reference inputs are at nearly the same voltage. Since the daughter boards contain a mix of analog and digital circuitry, the use of well-behaved (and therefore quiet) comparators was essential. Low, medium, and high threshold DC voltages are individually programmable for all channels in the entire system, and are provided by the TILE boards.

The discriminator subcircuit is designed to reset its threshold to ground after being triggered so that the trailing edge of its pulse is well-timed with respect to the zero-crossing point of the shaped analog signal. (After the detection of a zero-crossing, the threshold returns to its non-zero value.) Because the shaping circuitry is linear, mixer-shaper pulses of identical shape but different size will yield bipolar, shaped pulses whose zero-crossing times are independent of amplitude. Our hope was to use this fact to extract timing information, in addition to energy information, from the

calorimeter signals. The timing accuracy will be adversely affected by variations in calorimeter pulse shape, externally produced noise, and channel-to-channel variations in the components used to construct the daughter boards.

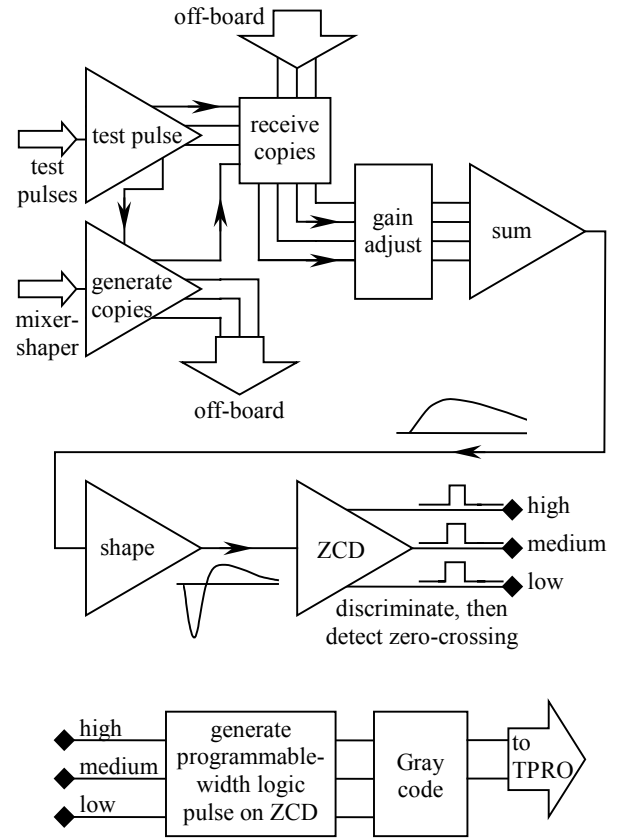


Figure 4: Functional diagram of a CLEO III daughter board.

The zero-crossing (trailing) edge of a discriminator signal triggers an output pulse generator built from a 74LS123 monostable multivibrator. The 74LS123's $R_{\text{ext}}/C_{\text{ext}}$ input is connected to a programmable current supply, instead of the usual resistor-tied-to- V_{CC} , allowing output pulse widths to be changed as desired.

The three thresholds' output pulses are priority-encoded to indicate the largest threshold achieved, converted to two-bit Gray code, then passed to the tile processor after being translated from TTL to LVDS levels. The use of Gray code, in combination with timing-related details of the priority encoding scheme, ensures that transient states of the outputs will not allow a medium threshold crossing to be mistaken for a high threshold crossing. Tile information formed by one daughter board usually corresponds to 64 crystals.

Test signals of programmable amplitude can be generated by a VME TILE board to excite any combination of the four analog inputs on a daughter board. A test pulse is created by differentiating a long TTL pulse using an 820 ns time constant (to mimic the light production by doped CsI), then feeding a current pulse with this time constant into a CsI preamp mounted on the TILE board. The signal passes through a copy

of the mixer-shaper signal path built onto the TILE board (which can adjust the size of the delivered test pulse using AD8842 TrimDACs), then arrives at the daughter board. Four AD8842 channels on each daughter board are used to further adjust the amplitudes of the mixer-shaper and three “intertile” test pulses. Since test pulses are fed into the differential amplifiers which receive each of the four “real” signals, the entire signal chain, including the daughter board’s input transistors, can be verified *in situ*. The TILE board contains a set of VME-readable latches which view all daughter boards’ digital outputs, and can be clocked a programmable interval after a test pulse is generated. By varying the test pulse amplitudes, signal path gains, discriminator thresholds, and latch delay relative to the test pulse, detailed studies of system behavior can be made in a non-invasive fashion whenever CLEO-III is not taking data.

An individual daughter board is powered with $\pm 12\text{V}$, $+5\text{V}$, -5.2V , and ground, consuming approximately 2 watts. Because a daughter board carries both analog and fast digital signals, care during board layout was necessary to avoid injecting noise into the analog circuitry associated with digital signals. To the greatest extent possible, signals were handled differentially. A detailed description of the entire analog section of the CLEO-III trigger, including schematics, a theory of operation, test procedures, photographs, and software lists is available on the Worldwide Web [9].

B. TILE VME board

As was previously mentioned, a TILE VME board provides power and ground to 24 daughter boards, as well as separately controllable DC levels used to define the high, medium, and low thresholds for each daughter board. Other DC levels, which can be set individually for each daughter board, are used to specify output trigger pulse widths. The sizes of test pulses generated on the TILE board can be adjusted using AD8842 TrimDACs, but each AD8842 controls one signal sent to a bank of six daughter boards. There are separate signal paths on the TILE board for test pulses routed to the mixer-shaper daughter board test inputs and “intertile” test inputs. (Four AD8842 channels on each daughter board were used to further adjust test pulse signals.)

Analog Devices AD9501 programmable delay generators are used to define an interval between the firing of a test pulse and the clocking of readback latches. The latches inspect the five digital signals generated by each daughter board: the outputs from the discriminators/zero-crossing detectors, as well as the two-bit Gray code trigger word. To our surprise, we discovered that the AD9501 is quite sensitive to noise on its digital input lines. In spite of this, we are able to achieve a shot-to-shot precision of about 25 ns in the test pulse - latch gate delay interval.

The TILE board includes the necessary VME interface, built mostly from field programmable gate array (FPGA) devices, required to allow us to communicate with the DAC’s. TrimDAC’s, readback latches, and delay generator chips used to configure and test the system through the VME backplane.

The trigger Gray code words generated by daughter boards are converted to LVDS (Low Voltage Differential Signal)

logic levels by TILE boards before being sent to the TPRO (tile processor) boards.

Since the TILE board routes the various analog signal copies between daughter boards, its layout also needed to be done with an eye towards the board’s mixed signal nature. Front panel connectors accepting twisted-pair ribbon cables are used to send copies of mixer-shaper signals (generated by daughter boards) across TILE board boundaries. A fully-loaded TILE board consumes about 55 watts, including the power provided to its 24 daughter boards. The trigger requires 16 (8) TILE boards loaded with 24 (15) daughter boards for barrel (endcap) crystals. Approximately 30 TILE boards were built for CLEO-III.

C. Quiet VME (QVME) Interface

In an effort to minimize noise in the trigger’s analog circuitry, all digital logic in the trigger’s four analog VME crates is disabled during data taking. We found that the MVME 2304 processors typically used in CLEO-III VME crates could inject an unacceptable amount of noise into a crate’s +5V power distribution. As a result, a “quiet VME” interface (QVME) was developed, allowing the processor which is used to configure and test TILE and daughter boards to be installed in a separate VME crate. The processor employs commercial IndustryPack parallel port modules to drive ribbon cables which carry VME address, data, and control lines information to the QVME in each analog crate. Only slightly more sophisticated than a cable connector, a QVME then places the appropriate signals on the crate’s backplane lines. The IP modules (two per QVME) reside on IP carrier boards in the same crate as the processor. Two such carriers, controlled by one processor, provide the configuration and control functions for all four of the analog calorimetry crates. The TILE boards employ a fairly conventional combinatoric (oscillator-free) VME interface which is able to load configuration data into the entire set of TILE and daughter boards in a few seconds.

D. Tile Processor (TPRO) and SURF boards

The tile processor (TPRO) boards can receive data from as many as 384 (overlapping) active tiles in the calorimeter barrel and 120 tiles in the endcaps. The first task of the tile processor is to filter event data so that overlapping, or adjacent, tiles which contain energy are reduced to a single hit. After filtering the data, the tile processor then determines the number of showers and their positions in the calorimeter. The CC trigger is expected to be most useful to CLEO-III for events in which the tracking trigger may be inefficient—typically events with a small number of tracks in a relatively quiet detector. Events with a large amount of activity in the detector will almost always satisfy the tracking trigger and are of less concern.

The algorithm run by the TPRO boards is a compromise between angular (and energy) resolution and the desire to limit the amount of information to be processed by the trigger. As shown in Figure 5, the boards remove all but the highest threshold tile in a group of contiguous, or overlapping, tiles. Calorimeter boundaries between TPRO boards are handled properly. Tile processor boards then project the two-

dimensional tile information into one-dimensional distributions in θ (parallel to the electron/positron beams) and ϕ (around the circumference of the calorimeter barrel). Since events with small amounts of detector activity are unlikely to be harmed by projection ambiguities, this proves to be an effective technique for producing a compact description of the number, positions, and energy levels of the showers.

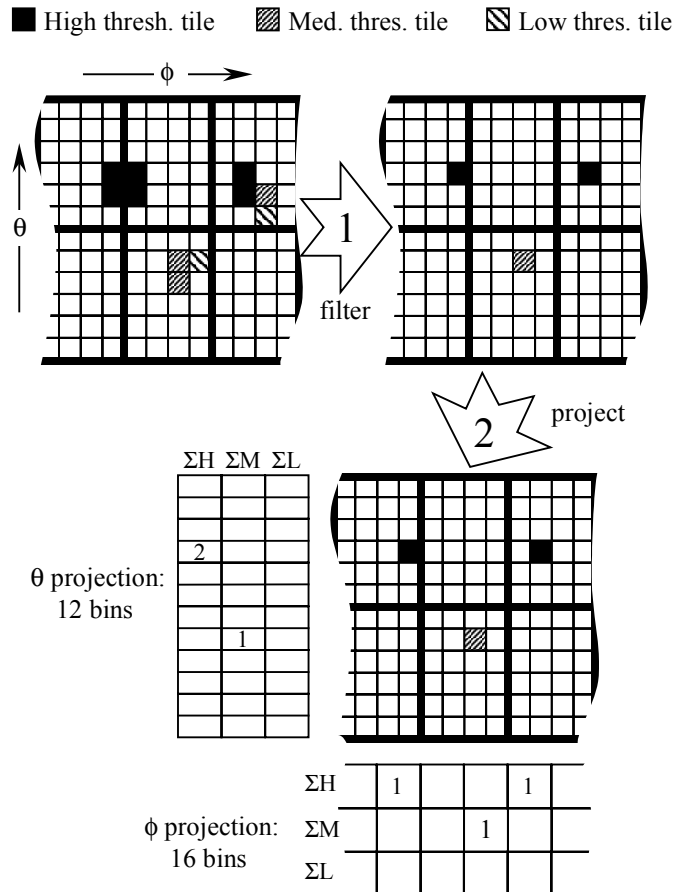


Figure 5: Steps for tile processing. 1. Filter contiguous tiled regions. (Barrel and endcap regions are similar.) 2. Project tiles in θ and ϕ ; sum, then pass information to the level 1 decision crate.

Four TPRO boards receive signals from the sixteen barrel TILE boards, while two process data from the eight endcap TILE boards. Processing is done in several pipelined 42 ns-duration stages. During the first stage, two sequential sweeps are made in which tiles that are near other tiles of equal or greater energy are removed. The details of the scheme ensure that no race-conditions occur, and that complicated patterns will, at worst, result in additional showers being reported rather than real showers being discarded. During the second 42 ns stage each processor produces the θ and ϕ projections of its remaining tiles as well as a cluster count for each of the three energy thresholds. Processors combine adjacent rows in the ϕ projections (finer granularity than this is not useful) so that the projections comprise 12 bins in θ and 16 in ϕ .

The TPRO boards use Altera EPF8820AQC160-2 FPGA's functioning in parallel to perform the bulk of their work. Each FPGA receives data from a single TILE board, so that one tile processor board is built around four Altera FPGA's.

Once the individual processors have produced their results, one SURF board combines the four barrel TPRO projections and tile counts. A second SURF board does the same for the endcap processors. The results are sent to the Level 1 decision electronics.

Since the TPRO processing pipeline is free-running, calorimeter event timing information comes directly from the fixed latency between calorimeter energy deposition and the propagation of the zero-crossing tile data through the tile processor.

IV. PROJECT STATUS

The calorimeter trigger was built, then installed at CLEO-III during 1999-2000. As of October, 2000 we are using it in a "non-shared" mode (in which we do not combine signals across daughter board boundaries) while we evaluate the system's noise immunity and timing properties.

V. SUMMARY

The calorimetry elements of the CLEO-III trigger have been presented. We have described the analog and digital circuitry used to draw conclusions about the pattern of energy deposition in the CLEO-III CsI electromagnetic calorimeter.

VI. REFERENCES

- [1] see also "The CLEO-III Trigger: Axial and Stereo Tracking" in these proceedings, Paper NSS576.
- [2] see also "The CLEO-III Trigger: Decision and Gating" in these proceedings, Paper NSS578.
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