XTRP - CLOCK/CONTROL

CLOCK & BUNCH ZERO HANDLING

L208/L2/SVT DATA HANDLING

PIPE FPGA

Phased Lock Loop

MPX

Shift Reg.

TEST CLOCK

Clock Control

Sync

FANOUT

XTRP 33ns Clk

XTRP 132ns Clk

XTRP Sync

XTRP B0

Crossing #

L1 Accept

FIFO WRITE & READ CONTROL

LEVEL 2 DECISION BUFFERS

L2 FIFO

L2 DATA OUT

L2 DATA

Phi Encoder

2:1 MPX

SVT FIFO

SVT DATA OUT

VME DATA OUT

L2 Accept

L1 Accept

Trailer Word

VME DATA BUS

132 Clock In

Receiver

Tap Delay Adj.

2 ns

Fine Adjust

Coarse Adjust

Radial distribution to all boards within crate via equal length traces on backplane.