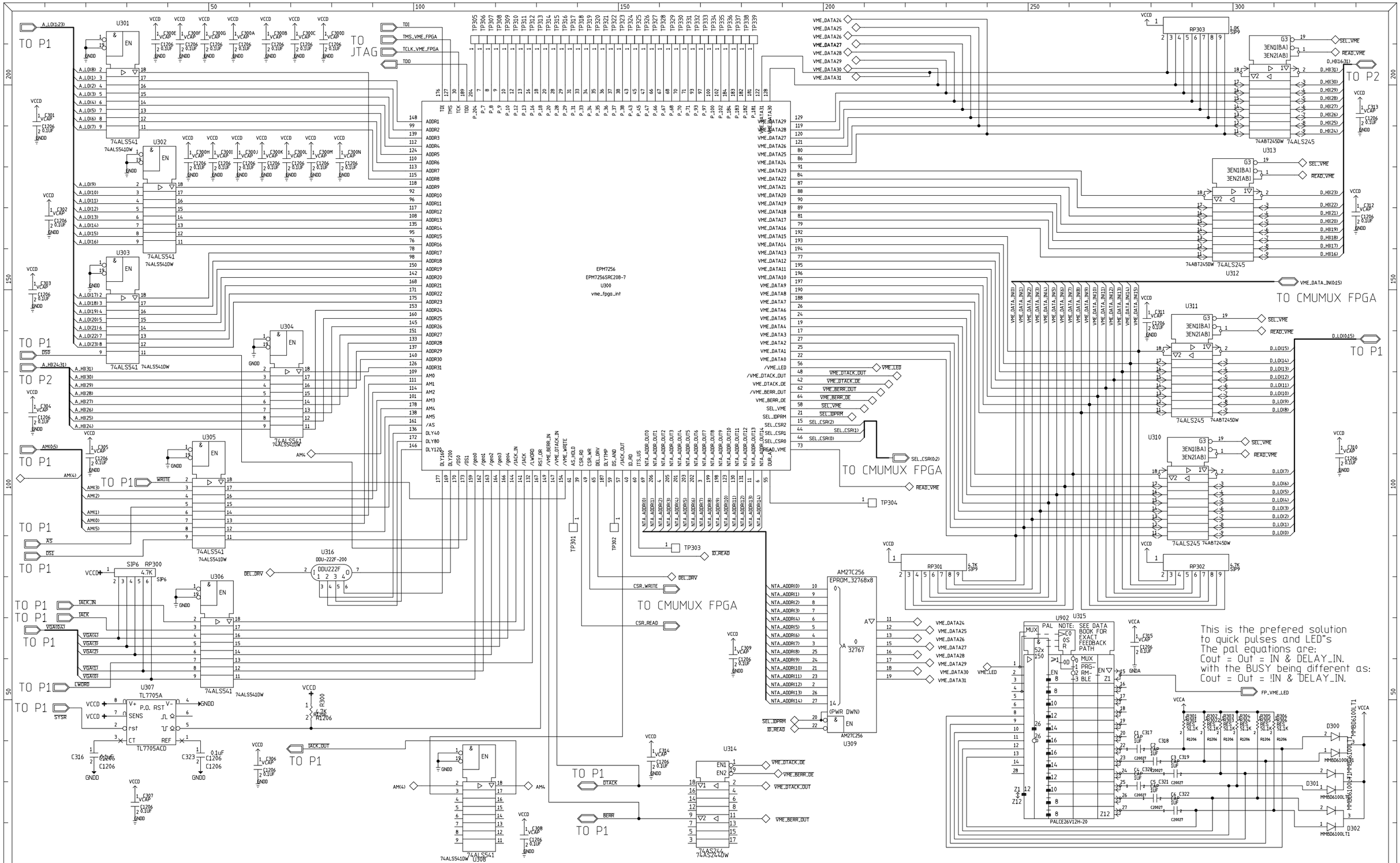
TO P1
TO P2
TO JTAG
TDI
TMS_VME_FPGA
TCLK_VME_FPGA
TDO
EPM7256
EPM7256SRC208-7
U300
vme_fpga_int
TO CMUMUX FPGA
TO CMUMUX FPGA
TO CMUMUX FPGA
VME_DATA_IN(0:15)
D_LO(0:15)
D_HI(16:31)
FP_VME_LED
This is the prefered solution
to quick pulses and LED"s
The pal equations are:
Cout = Out = IN & DELAY_IN.
with the BUSY being different as:
Cout = Out = !IN & DELAY_IN.
PAL NOTE: SEE DATA BOOK FOR EXACT FEEDBACK PATH
PALCE26V12H-20
AM27C256
EPROM_32768x8
74ALS541
74ALS541DW
74ALS245
74ABT245DW
74ALS244
74ALS244DW
TL7705A
TL7705ACD
DDU222F-200
MMBD6100LT1
HIGH ENERGY PHYSICS GROUP
HEPG
UNIVERSITY OF ILLINOIS URBANA - CHAMPAIGN
COPY OF DRAWING NO.:
DESIGNED BY: TODD MOORE
DATE DESIGNED: 9.1.99
USED ON:
TITLE: CDF CMU MUX VME INTERFACING CIRCUIT
FILE: VME
DRAWING NO.: C03/09
VME035
REV.:
DATE LAST REVISED: 4.12.01
HEPG SIZE B